Tutorial at NUiCONE 2017, Nirma University, Ahmedabad

Title: SoC-NoC Test Challenges

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Abstract: To handle design complexity and short time-to-market, it is increasingly common to use modular design approach in SoC. Such modules are called Intellectual Property Cores. Today's System on Chip (SoC) has been in true sense a Sea-of-Core (SoC) which contains a large amount of IP cores within it. The structure of such IP cores are often hidden from system integrator. Because of ready-made, black-box approach of IP does not allow any modification to its internal scan chain or any DFT insertion. Further, any testing tools like Automatic Test Pattern Generator (ATPG) or fault simulation cannot be applied to it. Such cores are coming with ready to use test data. This all points have made SoC testing very challenging. The first half of tutorial would begin with the introduction to IP Core based SoC covering need of IP Cores, types of IP cores, Today's SoC architecture and the issues being faced by SoC integrator. It will cover the fundamentals of IC

testing in brief. Finally, SoC test challenges in context of today's IP core based Design will be cover in length.

NoC option is becoming an important trend because of its advantages on tackling the challenges of a complex SoC design. However, to become a real standard or an industrial reality, it is important that the issues related to its testing are also well understood and dominated. Initially, the challenges to test and diagnose faults in NoCs are presented. A NoC is basically made up of three main components: network interface, routers and communication channels. The second half of tutorial covers various techniques used to test all these three components.