Proposal for Tutorial in

6th Nirma University International Conference on Engineering (NUiCONE 2017)

23-25 November 2017, Ahmedabad, India

by

Prof. Dr. P. N. Tekwani (*Senior Member – IEEE, Associate Editor – IEEE TIE*)

Professor and Head, Department of Electrical Engineering

Nirma University, Ahmedabad, India

(E-mail: pn.tekwani@nirmauni.ac.in)

Control Techniques for Multi-Level Inverters for Induction Motor Drives and Power Quality Improvement

In pulse width modulated (PWM) inverters, it has been a general practice to switch the power semiconductor devices at possibly high frequencies in order to shift the harmonic spectrum to higher frequency side. However, for the high-power industrial drives, voltage source inverter (VSI) operating at high switching frequencies are seldom preferred due to high switching losses. Multi-level inverter technology has emerged as a preferred solution for the high-voltage high-power industrial induction motor (IM) drive applications. As the output voltage waveforms of a multi-level inverter consists of smaller multi-stepped amplitudes, the resulting *dv/dt* at the motor inputs is less and the electromagnetic interference (EMI) caused by the switching is considerably reduced. Hence, inverter systems of high voltage levels can be easily built-up using the existing switching devices of lower voltage ratings. Multi-level inverters can greatly reduce the harmonic content in output voltage waveforms, enabling them to be operated at much lesser frequencies, resulting into much lesser switching losses.

Current-Controlled PWM (CC-PWM) VSIs are extensively employed in high performance drives (HPD) because of the considerable advantages offered by them, such as, excellent dynamic response and inherent over-current protection, as compared to the voltage-controlled PWM (VC-PWM) VSIs. Amongst the different types of CC-PWM techniques, hysteresis current controllers offer significant simplicity in implementation. However, conventional type of hysteresis controllers (with independent comparators) suffers from some well-known drawbacks, such as, limit cycle oscillations (especially at lower speeds of operation of machine), overshoot in current error, generation of subharmonic components in the current, and random (non-optimum) switching of inverter voltage vectors.

Tutorial will focus on current error space phasor based hysteresis controller for three-level VSI fed IM drives, active power filters and unity power factor front-end converter. The scheme does not need computation of machine back emf vector and information on the same is indirectly derived from the direction and amplitude of current error space phasor. Current error space phasor is kept within the hexagonal boundary by selecting appropriate inverter voltage vector, using a simple look-up table. The controller always selects one of the three adjacent inverter voltage vectors forming a triangular sector, in which, the tip of machine voltage vector lies. The scheme is self-adaptive for any possible amplitude and position of machine voltage vector, and provides smooth transitions of inverter output voltage levels, up to the twelve-step mode of operation. All the advantages of conventional hysteresis controllers are retained in the proposed scheme. The scheme can be applied to any inverter configuration that generates three-level voltage space phasor structure.

Common problems associated with the conventional, as well as current error space phasor based hysteresis controllers with fixed bands (boundary), are the wide variation of switching frequency in the fundamental output cycle and variation of switching frequency with the change in speed of the load motor. These problems cause increased switching losses in the inverter, non-optimum current ripple, excess harmonics in the load current and subsequent additional machine heating. Tutorial will focus on current error space phasor based simple hysteresis controller for controlling the switching frequency variation in two-level PWM inverter fed IM drives. A parabolic shape of the boundary for current error space phasor is reported. A novel concept of on-line variation of this parabolic boundary, depending on motor speed, is suggested to obtain switching frequency spectrum similar to that of the constant switching frequency VC-SVPWM (space vector PWM) based VSI fed IM drive. A simple generalized algorithm is also described for determining the set of parabolic boundaries for controlling the switching frequency variation for a two-level inverter feeding any given induction motor. Sector change logic is self-adaptive and is capable of taking the drive up to six-step mode, if needed. All other inherent advantages of space phasor based hysteresis controller are retained in the proposed scheme, in addition to control of switching frequency variation with optimum PWM switching.

Similar to the conventional two-level PWM inverters, different topologies of multi-level PWM inverters also generate alternating common-mode voltage (CMV) in the IM drive system. This alternating CMV, coupled through parasitic capacitances of the machine windings and frame, can result in shaft voltages and consequent excessive bearing currents in the IM drive system. Frequent repetition of these bearing currents causes electric discharge machining (EDM) phenomenon, which leads to premature failure (pitting and fluting) of motor bearings.

This CMV also adds to the total leakage current through ground conductor, which acts as a source of conducted EMI in the IM drive system and causes malfunctioning of electronic equipment and false tripping of relays. A five-level inverter topology, with switching state combination selection strategy for PWM control, will be discussed for complete elimination of alternating CMV in the entire operating range of the IM drive, including over-modulation up to 24-step mode of operation. Proposed scheme is based on a dual five-level inverter fed open-end winding IM drive, which results in a nine-level inverter voltage space phasor structure with the presence of alternating CMV. Individual five-level inverter is formed by cascading a three-level neutral point clamped (NPC) inverter with two conventional two-level inverters. Thus, it offers modular and simple power bus structure with reduced power diode count as compared to that of a conventional five-level NPC inverter. The present open-end winding IM drive needs nearly half the dc-link voltage and offers more number of redundant switching state combinations as compared to a single five-level inverter fed conventional IM drive. When only those voltage vectors of the individual five-level inverter, which do not generate alternating CMV at the inverter poles, are exclusively used for switching the dual inverter, then a five-level inverter voltage space phasor structure with zero CMV in the machine phase voltage is achieved. With the absence of CMV in the drive, both the five-level inverters can be fed from common dc-links without generating any zero sequence current. Hence, the proposed drive needs only four isolated dc power supplies.

Inherent unbalance in the dc-link capacitor voltages of NPC multi-level inverter (supplied with a single dc power supply) produces lower order harmonics at inverter output, torque pulsation and increased voltage stress on power switching devices. A dual five-level inverter fed open-end winding IM drive with two dc power supplies is proposed to achieve the dual task of CMV elimination and dc-link capacitor voltage balancing. Dependency of the divergence in dc-link capacitor voltages on the dc-neutral currents is mathematically analysed. Conditions to maintain the voltage balance in all the four capacitors of the dc-link are also established. An open-loop control scheme is presented, which uses only the availability of redundant switching states for inverter voltage vectors. The proposed open-loop scheme is inherently capable of maintaining the existing dc-link capacitor voltage balance in association with CMV elimination in the entire operating range, irrespective of the load power factor. The limitation of the proposed open-loop control scheme, to take corrective action towards unbalanced capacitor voltage, is further investigated using a closed-loop control scheme. The unbalance in capacitors voltages is sensed and the switching state combinations, which can provide corrective action for that, are appropriately switched. Voltage balancing is achieved, without affecting the output fundamental voltage, by effective utilization of redundant switching states. The proposed closed-loop controller achieves simultaneous elimination of CMV and dc-link capacitor voltage unbalance in the entire linear and over-modulation range (up to 24-step mode operation) of the drive, in motoring as well as in regenerative modes.

All the above investigations will be discussed with extensive simulation results and experimental results obtained on laboratory prototypes. All the control schemes are implemented digitally on a digital signal processing (DSP) platform (TMS320F240/2407A). Experimental results will be presented along with the simulation results, showing a close agreement between them. It will be quite interesting for researchers working in this areas to see the applications of multi-level inverters in induction motor drives, active power filters and IGBT based front-end bi-directional converters.

Prof. Dr. P. N. Tekwani
Young Associate - Indian National Academy of Engineering (INAE),
Senior Member - IEEE, Senior Member - IEEE Industrial Electronics Society (IES), Associate Editor – IEEE TIE
Member - The Institution of Engineers (India) – (IEI),
Life Member - Indian Society for Technical Education (ISTE), Life Member - Society of Power Engineers (India),
Rajarambapu Patil National Award - 2016 for the Promising Engineering Teacher
ISTE-CVM Award - 2014 for Best Engineering College Teacher in Gujarat State
ISTE-L&T National Award - 2011 for Guiding Best M.Tech. Thesis in the Electrical & Electronics Engineering
IEI Young Engineer National Award 2010-2011
ISTE-SGSITS National Award - 2009 for Research Work done by Young Teacher
Young Engineer National Award - 2008 of INAE (Indian National Academy of Engineering)
Best Engineer "Mylavaram" Award - 2001 for Excellence in Work - ERDA
Ph.D. (Power Electronics), CEDT, Indian Institute of Science (IISc) Bangalore
“Tag Corporation Medal” Award for Best Ph.D. Thesis
M.E. Electrical Engineering (Industrial Electronics), M. S. University of Baroda, First Rank
B.E. Power Electronics, Saurashtra University, University First, Gold Medalist
Head of the Department, Section Head and Professor of Electrical Engineering
Coordinator of PG Electrical Engineering (Power Electronics, Machines & Drives) Programme
Department of Electrical Engineering,
Institute of Technology, Nirma University, Sarkhej-Gandhinagar Highway, AHMEDABAD – 382 481, GUJARAT, INDIA
e-mail: pn.tekwani@nirmauni.ac.in
Phone (office): 0091-2717-241911-15 (Extn.: 401), Direct: 0091-79-30642401, Fax: 0091-2717-241917